WHAT IS CLAIMED, IS

1. A video apparatus with a digital decoder having a first memory on an internal bus and linked to an OSD circuit and to a second memory via a main bus,

the video apparatus comprising means for realising a DMA transfer between the first memory and the second memory.

2. A video apparatus according to claim 1, wherein a CPU is connected to the main bus.

3. A video apparatus according to claim 2, wherein the second memory is used by the CPU.

4. A video apparatus according to claim 1, wherein the first memory is a Video RAM and wherein the second memory is a CPU RAM.

5. A video apparatus according to claim 1, wherein the digital decoder is connected to a digital front-end.

6. A process for controlling a video apparatus with a digital decoder having a first memory on an internal bus and linked to an OSD circuit and to a second memory via a main bus,

comprising the step of realising a DMA transfer between the first memory and the second memory via the digital decoder.

7. A process according to claim 6, comprising the following steps :

- issuing a request for the OSD circuit to use more than a given size in the second memory,
- realising a DMA transfer from the second memory to the first memory.
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8. A process according to claim 7, with the further steps of :

- issuing a request for the OSD circuit to use data in the first memory,
- copying via a DMA transfer data from the second memory to the first memory ;
- realising a DMA transfer of the requested data from the first memory to the second memory.